Development of a Real-Time, High-Frequency Ultrasound Digital Beamformer for High-Frequency Linear Array Transducers

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Abstract—A real-time digital beamformer for high-frequency (>20 MHz) linear ultrasonic arrays has been developed. The system can handle up to 64-element linear array transducers and excite 16 channels and receive simultaneously at 100 MHz sampling frequency with 8-bit precision. Radio frequency (RF) signals are digitized, delayed, and summed through a real-time digital beamformer, which is implemented using a field programmable gate array (FPGA). Using fractional delay filters, fine delays as small as 2 ns can be implemented. A frame rate of 30 frames per second is achieved. Wire phantom (20 μm tungsten) images were obtained and -6 dB axial and lateral widths were measured. The results showed that, using a 30 MHz, 48-element array with a pitch of 100 μm produced a -6 dB width of 68 μm in the axial and 370 μm in the lateral direction at 6.4 mm range. Images from an excised rabbit eye sample also were acquired, and fine anatomical structures, such as the cornea and lens, were resolved.

I. INTRODUCTION

HIGH-FREQUENCY (>20 MHz) ultrasound has demonstrated high spatial resolution on the submillimeter level, and has been successfully applied to ophthalmology [1]–[3], dermatology [4]–[6], small animal imaging [7]–[9], and intravascular imaging [10]. These applications, however, used only single-element transducers, which are mechanically scanned to form an image. The single-element transducers can provide focus only in a limited region, and a low frame rate because of the mechanical motion. Although B-mode/depth (B/D) scan can provide a more extended focal region [5], [6], the consequence is a decrease in the frame rate and an extra movement in the axial direction, which make the imaging system more susceptible to motion artifacts.

Compared to single-element transducers, linear arrays allow for dynamic focusing that improves the lateral resolution throughout the depth of view and electronic scanning that provides high frame rate. Furthermore, the handheld operation and lack of scanning motion of linear array imaging systems are more clinically convenient, safer, and more reliable. However, linear array design requires an element pitch, defined as the distance between the centers of two adjacent elements, to be less than one ultrasound wavelength in order to fully suppress grating lobes [11]. This brings great difficulties to the fabrication of high-frequency linear array transducers when the ultrasound wavelength is only approximately 50 μm at a frequency of 30 MHz, for example. Moreover, the relatively small elements in a linear array have higher electrical impedance resulting in poor sensitivity. And the beamforming electronics are not yet commercially available due to cost and complexity [12], [13]. All of these difficulties have prevented the widespread fabrication and application of the high-frequency linear arrays. Nevertheless, Ritter et al. [12] developed the first 30 MHz, 48-element linear array transducer with a 100 μm pitch using piezocomposite material. Cannata [13] reported the fabrication of a 35 MHz linear array with a 50 μm pitch, which is the highest frequency medical imaging capable linear array fabricated to date.

It is equally challenging to develop a high frequency ultrasound imaging system. A number of schemes have been reported for imaging using linear arrays or phased arrays [14]–[20]. A system prototype for a 20–25 MHz linear array was reported where only five elements were used in the active subaperture [14]. A 20-MHz, 64-element circular array for an intravascular application was developed with integrated front-end circuitry, and the images were obtained using a synthetic aperture approach [18], [19]. Stitt et al. [20] developed a 16-channel analog beamformer for a 30 MHz linear array built by Ritter et al. [12]. The architecture of this beamformer is bulky and has a relatively low frame rate (10 frames per second). It has to be miniaturized and the frame rate increased to have any practical application. There are several hurdles that have to be overcome in the development of a high-frequency imaging system. High-speed and wide bandwidth electrical components are necessary for high-frequency imaging. Higher computation power and large data storage capability are desired for a real-time beamformer. Noise tolerance is stricter for high-frequency arrays because of the higher attenuation.

A 16-channel FPGA-based real-time digital beamformer has been developed. The digital beamforming is implemented inside the FPGA for the digitized echoes from 16 adjacent transducer elements. The hardware architecture of the design provides great flexibility for beamforming, such as dynamic receive focusing and receive apodization. Due to the high clock rates (maximum is 400 MHz...
for the Xilinx FPGA XC2VP20, (Xilinx, Inc., San Jose, CA), reprogrammability, and flexibility, FPGAs are an ideal platform for developing the beamformer, and have been successfully applied to digital beamformers. Examples of FPGA beamformer implementations include a system for the 5 MHz center frequency linear array [21] and a system for the 50 MHz center frequency annular array transducer [22], [23]. For a high-performance imaging system both dynamic focusing in transmit and receive at all location is necessary, but considering the complexity of circuit design and frame rate (real-time), the first generation design is implemented with only dynamic focusing in receive.

This paper reports the progress that has been made in the development of a prototype real-time FPGA-based digital beamformer for high-frequency linear arrays. The design and how it was implemented is described. Images from wire targets (20 µm diameter tungsten wires) were used to assess both axial and lateral resolutions of the system. Real-time images from an excised rabbit eye were acquired, demonstrating the feasibility of using high-frequency linear array to image the region of interest, such as cornea, lens, and iris.

II. SYSTEM HARDWARE

The imaging system consists of a computer for displaying the image, a 16-channel FPGA-based beamformer, a 16-channel analog variable gain amplifier (VGA) and time gain compensation (TGC) amplifiers, a 16-channel transmit focusing control, a 64-channel receive, and a 30 MHz linear array. The main concern of the system design is to digitize the 16-channel radio frequency (RF) data, and process the acquired data fast enough for real-time imaging.

As shown in the system diagram (Fig. 1), the computer serves as the user interface. Upon each frame trigger sign given by the computer, the microprocessor inside universal serial bus (USB) (CY7C68013, Cypress Semiconductor Corp., San Jose, CA) sequentially sends out trigger signals to other blocks. The line trigger is first delivered to the 16-channel transmit focusing control, which consists of three SX52BD (Ubicom Inc., Mountain View, CA) high-speed microcontrollers. The microcontrollers are used as the central timing controller for transmit focusing. They send the trigger signals to the pulsers, and control signals to the demultiplexers which connect the transducer elements to the 16-channel transceiver. Coaxial cables are used to connect transceiver with linear array. The amplified echoes are first digitized using 16 8-bit analog-to-digital converts (AD9054A, Analog Devices, Inc., Norwood, MA) at 100 MHz and then aligned by an FPGA (XC2VP20-6FF896C, Xilinx, Inc.) based beamformer. The delay of the beam data is implemented in two steps: coarse delays, which are integer multiples of the clock period, are obtained by the coarse delay unit and finer delays less than one clock period are processed by fractional delay filters. The beamformed data then is transferred to a computer through the USB port for real-time display (30 frames per second). A graphical user interface (GUI) software is developed using Visual C++ (Microsoft Corp., Redmond, WA) for real-time display.

A. Analog Front-End Circuit

The analog front-end circuit consists of three boards: a 64-channel transceiver board; a 16-channel, three-stage amplification board; and a transmit focus circuit board.

The transceiver board is triggered by 16, 5-volt, rising-edge signals. The signals pass through 16 1-of-4 demultiplexers (74AC139, National Semiconductor Inc., Santa Clara, CA) so that 16 adjacent elements are chosen. Triggered by these rising-edge signals, the pulser circuit generates a −66 volt impulse of 10 ns duration for each chosen element. Immediately following the transmitter/receiver (T/R) switch, 16 4-to-1 multiplexers (AD8184, Analog Devices Inc.) are used to select the corresponding activated element out of 64 elements. The 16 preamplifiers (MAX4107, Dallas Semiconductor Corp., Dallas, TX), an ultra low-noise Op Amp with a gain of 10 dB and a bandwidth of 200 MHz, are used to amplify signals. The demultiplexers and multiplexers are controlled by the same control signal to maintain the synchronization.

A three-stage, 16-channel amplification board, including one fixed gain amplifier, a TGC amplifier and a variable gain amplifier, provides another 30 to 70 dB gain to the echoes. Two AD603 are involved in the TGC and the gain-adjustable amplifier. A passive band-pass filter with the −3 dB cutoff frequency from 10 MHz to 50 MHz is used directly after second stage AD603. Before the signals are fed into the analog-digital converters (ADCs), a high-speed 16 × 16 video crosspoint switch (AD8114, Analog Devices Inc.) is used to rearrange the order of the analog outputs.

The transmit focusing circuit board provides 16 trigger signals with a minimum delay increment of 2 ns between pulsers. Three independent microprocessors (SDX52, Ubicom Inc.) are used in this design. The first microprocessor generates control signals to transmit demultiplexers and receive multiplexers. The second microprocessor sends out 16 triggers to 16 programmable delay chips (PDU13F-2,
Data Delay Device, Inc., Clifton, NJ) for transmit focusing. The delay chips provide maximum 14 ns delay with increment of 2 ns. Therefore, the transmit focusing delays are achieved in two steps: the integer multiples of 10 ns part of delays are fulfilled by software (using NOP instruct in software) and the delays less than 10 ns are implemented by controlling the PDU13F-2. The third microprocessor controls the 16 × 16 video crosspoint switch. Immediately after the first and the third microcontroller send out the signals, they will trigger the “ready” signal to the second controller. The second microcontroller, in turn, triggers the pulser circuitry.

B. Receive Delay Implementation

Although digital beamformers have been successfully used in conventional array imaging, there are still some practical challenges for high-frequency, ultrasonic transducer arrays: higher sampling rate is needed to adequately satisfy Nyquist criteria and obtain finer delays, and precision A/D converters are needed to capture all of the information in the array frequency range [24], [25]. The sampling rate should be 4–10 times higher than the array frequency as a rule of thumb so that the signals are adequately sampled to preserve echo information [25]. Because the linear array transducers used in this study have center frequencies in the 30 MHz range, A/D converters should operate in the range of 120–300 MHz in order to satisfy this criteria. However, considering the upper limit of all the electronic components, real-time imaging capability and the system complexity, our first generation of digital beamformer uses a 100 MHz sampling rate with digital interpolation filters, which allow the signals to be sampled at a lower frequency [26]–[28], while achieving finer delays. Using the 100 MHz sampled data, the fractional-delay interpolation is used to generate a fine delay from 2 to 8 ns with the increment of 2 ns inside the beamformer. This works by dividing the required delay into an integer number (M) of sample periods and a fraction (α) of a sample period. The fractional delay is introduced below. A detailed description of implementation of coarse and fine delays is given in the next section. All digital receive delays are implemented inside the FPGA.

A delay resolution as fine as possible is desired in order to obtain a well-focused beam; however, the delay increment is related to the complexity of the interpolation filter. After considering the tradeoff, a 4-tap FD FIR filter, with a delay resolution down to 2 ns, is chosen. A good review of the time domain FD filter design methods can be found in [28]. In this study, we used the classical Lagrange interpolation formula:

\[
h(n) = \prod_{k=0}^{N} \frac{\alpha - k}{n - k} \quad n = 0, 1, 2, \ldots, N, \tag{1}
\]

where \(N\) is the order of the filter, \(n\) is the index of the filter coefficient, and \(\alpha\) is the fractional value. In this design, the \(\alpha\) is 0.2 in order to obtain the 2 ns.

In order to evaluate the performance of the fractional delay, six echoes, sampling at 1 GHz, were generated using FIELD II (Jensen, Technical University of Denmark, Denmark) with a center frequency of 30 MHz and 50% bandwidth. It was assumed that the echo from each channel was identical. Those ideal echoes then were resampled at 100 MHz, taking one sample out of 10 samples to be considered as ideal waveforms as shown in Fig. 2(A). The resampled echoes are displayed with relative delays so that the first echo represents the echo received by center element, and the last one the echo by outermost element. Fig. 2(B) shows the comparison of the ideal summation that is the addition of the aligned ideal signals at the sampling rate of 1 GHz, and the summation of the filtered echoes which is the addition of the resampled 100 MHz data after they are aligned using fractional delay filters. It can be seen from Fig. 2(B), the results of the beamformer using the fractional delay filters is in good agreement with the ideal case.

C. Digital Beamformer Circuit

A combination of coarse and fine delay strategy is adopted in this study. The coarse delay, which is an integer multiple of the clock period, is accomplished by using a programmable delay unit structure; a 4-tap FD FIR filter generates fine delays less than one clock period. The beamformer in this system is implemented inside a Xilinx VirtexII series FPGA chip, where the FPGA has 564 I/O pads, and 1584 KB of RAM.

The coarse delay is implemented using the structure shown in Fig. 3. The time interval between two samples is dictated by the sampling rate. In this study, the 100 MHz ADCs are used and the clock period is 10 ns. One bit in the 4-bit delay coefficients (B4B3B2B1) controls the condition
of each multiplexer, which in turn decides if the data need delay or not. For example, if a delay of 60 ns is needed, the corresponding 4-bit delay coefficient is '0110'. The first multiplexer is '0', which means data will not flow over the 8 clock delay unit. Therefore, total delay in the data path is 40 ns + 20 ns = 60 ns. All delays, less than 16 clock cycles, can be expressed by \( B_4 \times 8 + B_3 \times 4 + B_2 \times 2 + B_1 \times 1 \). This can be extended to delay larger than 16 clock cycles by adding one more bit in the binary coefficient.

The fine delay is implemented using the structure illustrated in Fig. 4. The distributed arithmetic FIR filters, which use full-parallel, fixed coefficient, finite impulse response (FIR) digital filter structures, are used to implement a fine delay from 2 ns to 8 ns. Immediately after those filters, a 8:1 bus multiplexer is used to select the fine delay according to the delay coefficient. For both the coarse delay and fine delay, the delay coefficients are pre-calculated and stored in the state machine.

In the present design, the beamformer block diagram with dynamic receive focusing is shown as Fig. 5, which only shows the eight channels due to the symmetry of the delay values for 16 adjacent elements. The dynamic focusing procedure is performed by updating the receive delay for different focus depth. Instead of calculating the delay coefficients in real time, the calculation results are stored in FPGA and are updated in time according to the depth of the echoes. The transition between two states is triggered by a 10-bit counter. Because this structure is reconfigurable, dynamic receive focusing can be implemented with integer multiples of 0.5 mm step. In this study, 16 states are used so that the maximum depth for dynamic focusing is 8 mm if the increment is 0.5 mm. The final beam data is obtained by summing up the output from the FD filters.

Considering the possible communication interfaces between external devices and the computer, the RS-232 has lower data transferring rate whereas ISA and PCI are more complex and space limited for a multichannel board even though they provide very fast transferring speed. The USB is more advantageous for this study. It is of higher speed (<480 Mbps) and lower cost while possessing a simpler structure. In this design, an EZ-USB FX2™ USB Microcontroller and high-speed USB Peripheral Controller, is used to transfer data from the digital board to the computer. The flow chart of the software is shown in Fig. 6(A). The computer programming GUI has been developed with Microsoft’s Visual Studio Version 6 (Microsoft Corp., Redmond, WA). This GUI was designed to control the imaging system in the Windows platform. All the synchronization controls were integrated into the GUI menu [Fig. 6(B)].

Photographs of the completed electronic boards shown as Fig. 7 are the transmit focus circuit board; the 16-channel, three-stage amplification board; the 64-channel transceiver board; and the 16-channel digital beamformer board, respectively.

By electronically moving the active subaperture along the array one element away from the previous subaper-
Fig. 6. The flow chart of the firmware developed for FX2 (A), and the flow chart of the data acquisition software for computer (B).

Fig. 7. The photograph of the PCB boards. (A) The transmit focus circuit board. (B) The 16-channel, three-stage amplification board. (C) The 64-channel transceiver board. (D) The 16-channel digit beamformer board.

Fig. 8. Wire phantom (20 μm Tungsten) image from 30 MHz, 48-element linear array with the pitch of 100 μm. The image has the 25 dB dynamic range.

Cross-sectional images were obtained from a wire-target phantom. The phantom consists of 4 of 20 μm diameter tungsten wires (California Fine Wire Co., Grover Beach, CA) and arranged diagonally with lateral distance of 1.55 mm and axial distance of 0.65 mm. The wire phantom images using both 30 MHz linear arrays are shown in Fig. 8. All four wires are clearly resolved for both linear arrays. The −6 dB width for the 30 MHz array are measured to be 68 μm and 370 μm in axial and lateral direction from the wire in focal point (6.4 mm) in Fig. 8. The measured −20 dB width in lateral direction is 1.2 mm, and the simulation results show a value of 0.84 mm.

The excised rabbit eye image in vitro was acquired by placing the anatomy of interest (specifically the cornea and lens) near the transmit local point. The active subaperture of the array was electronically scanned across the eyeball. For the 30 MHz array with 48-element, the width of the field of view in azimuthal direction is 3.3 mm. The eyeball image is shown in Fig. 9. The anterior region, consisting of structures such as cornea and lens, is resolved.

III. Experimental Results
In this paper, a digital FPGA-based, real-time, high-frequency beamformer was presented. The 16-channel beamformer is implemented in one FPGA chip, which reduces hardware complexity. The 30 MHz, 48-element array with a pitch of 100 $\mu$m was used to acquire the experimental images of wire targets and excised rabbit eyeball. The results showed that the 30 MHz array has the $-6$ dB width of 68 $\mu$m in axial and 370 $\mu$m in lateral direction at 6.4 mm. Images from an excised rabbit eye sample also were obtained, and fine anatomical structures were observed.

IV. Conclusions

In this paper, a digital FPGA-based, real-time, high-frequency beamformer was presented. The 16-channel beamformer is implemented in one FPGA chip, which reduces hardware complexity. The 30 MHz, 48-element array with a pitch of 100 $\mu$m was used to acquire the experimental images of wire targets and excised rabbit eyeball. The results showed that the 30 MHz array has the $-6$ dB width of 68 $\mu$m in axial and 370 $\mu$m in lateral direction at 6.4 mm. Images from an excised rabbit eye sample also were obtained, and fine anatomical structures were observed.

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Fig. 9. The ex vivo anterior chamber section image of an excised rabbit eye using the 30 MHz linear array. The image has the 25 dB dynamic range.
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