Lecture 5: Super Pipelining

Superscalar Pipelines

1. Only one instruction enters the pipeline per clock
   - Remember IRON LAW = CPI * code size * frequency
   - CPI = 1 for the 5-stage pipeline

2. When we unified instructions some stages were too inefficient
   - EX is forced to be one stage, but MULT and ADD have different execution latencies
   - Every instruction spends the same time in EX stage

3. Instructions stall whenever there is a dependence and data cannot be forwarded in time
   - Even worse, unnecessary stalls for instructions that are not even waiting for data
   - Solution: Out-of-order Execution

Intel Pentium Parallel Pipeline

- Superscalar pipeline with width of 2
- Essentially clones 486 5-stage pipeline
- Then separate execution pipeline into two cases
  - U pipe is universal instruction handler
  - V pipe handles most but not all instructions
- Pipeline diversification to improve efficiency
  - Still an in-order pipeline
- Cost
  - Doubles required resources
  - Decoders, register ports, memory ports
  - Uses 8-way interleaved cache to approximate dual ported cache

Diversified Pipelines

- Specialized pipeline to handle different instruction types
  - Most first generation CPU used FP and INT pipelines
- New problems arise, let us now look at class notes 40-46

Power4 Diversified Pipelines

- Introduced in 2001 at 1.3 GHz
- Cluster of two INT/LD, one FP, one BR units
- We will study various units shown in this figure later!