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Lecture 5: Super Pipelining Superscalar Pipelines

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Lecture notes based in part on slides created by Michel Dubois,
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 and Jim Smith

3 Limitations of 5-stage Pipeline

- Only one instruction enters the pipeline per clock
 - Remember IRON LAW = CPI * codesize * frequency
 - CPI = 1 for the 5-stage pipeline
 - Solution: Superscalar pipelines (multiple instructions/clock)
- When we unified instructions some stages were too inefficient
 - EX is forced to be one stage, but MULT and ADD have different execution latencies
 - Every instruction spends the same time in EX stage
 - Solution: Diversified Pipelines
- Instructions stall whenever there is a dependence and data can not be forwarded in time
 - Even worse, unnecessary stalls for instructions that are not even waiting for data
 - Solution: Out-of-order Execution

Superscalar Pipelines

Non-pipelined machine
 Scalar Pipelines
 Every clock many things happen

Pipelined & Parallel Execution
 Every clock many copies execute and many things happen: Superscalar pipelines

(a) No Parallelism (b) Temporal Parallelism (c) Spatial Parallelism (d) Parallel Pipeline

Non-Pipelined but Parallel Execution
 Every clock many copies execute
 Needs more hardware

Intel Pentium Parallel Pipeline

- Superscalar pipeline with width of 2
- Essentially clones 486 5-stage pipeline
- Then separate execution pipeline into two cases
 - U pipe is universal instruction handler
 - V pipe handles most but not all instructions
 - Pipeline diversification to improve efficiency
- Still an in-order pipeline

Cost

- Doubles required resources
 - Decoders, register ports, memory ports
- Uses 8-way interleaved cache to approximate dual ported cache

Diversified Pipelines

- Specialized pipeline to handle different instruction types
 - Most first generation CPU used FP and INT pipelines
- New problems arise, let us now look at class notes 40-46

Power4 Diversified Pipelines

- Introduced in 2001 at 1.3 GHz
- Cluster of two INT/LD, one FP, one BR units
- We will study various units shown in this figure later!